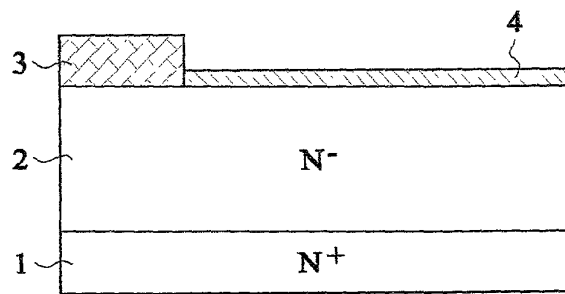
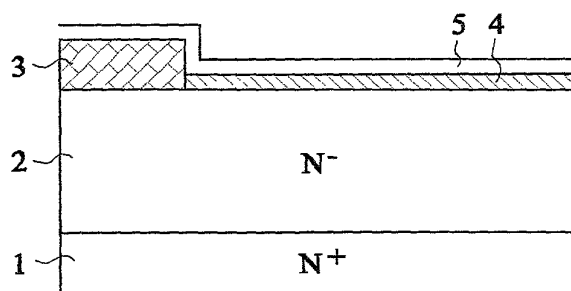


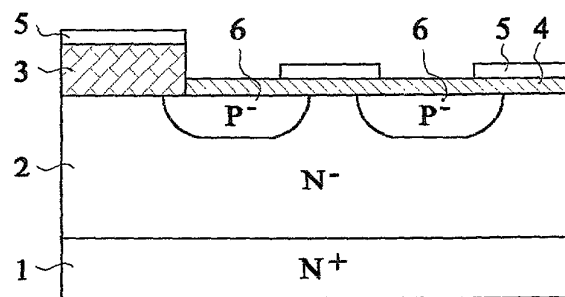
(a)



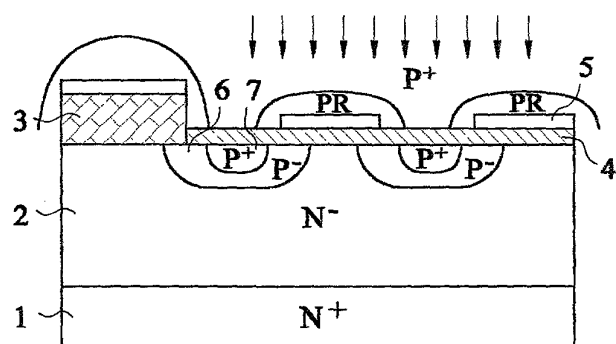
(b)



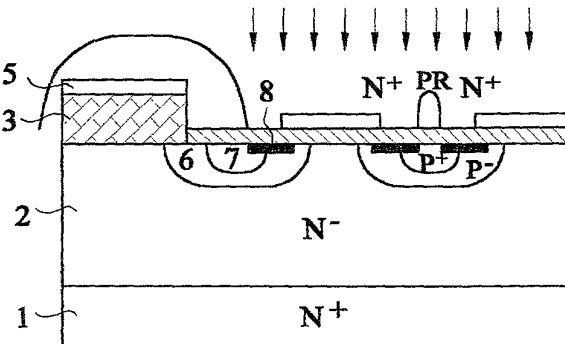
(c)



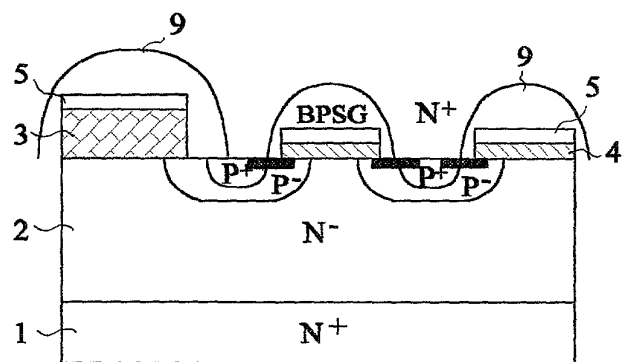
(d)



(e)



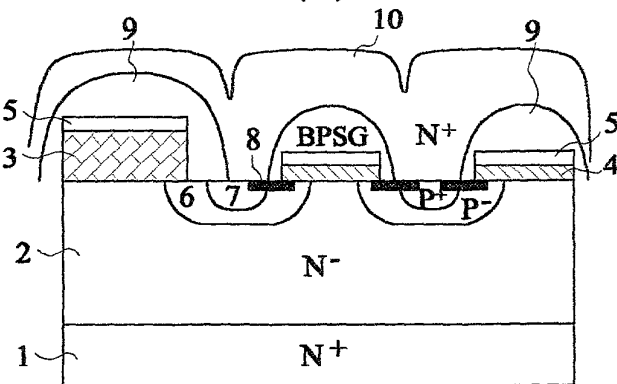
(f)



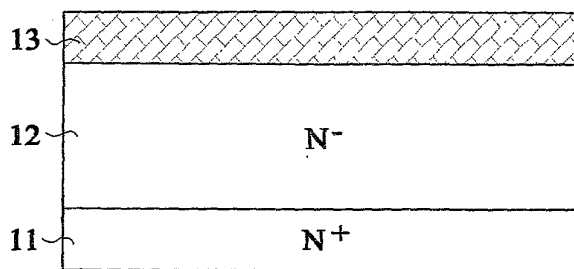
(g)

(PRIOR ART)

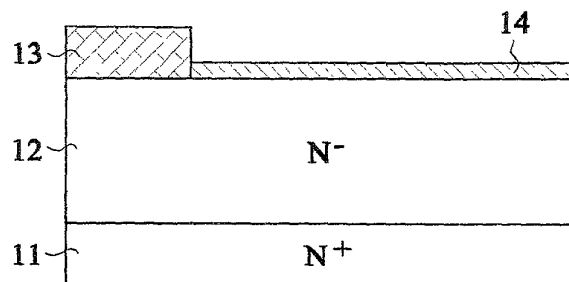
FIG. 1



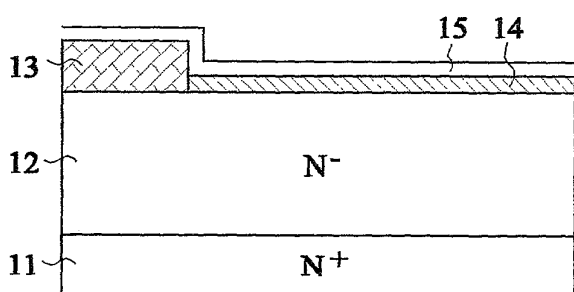
(h)



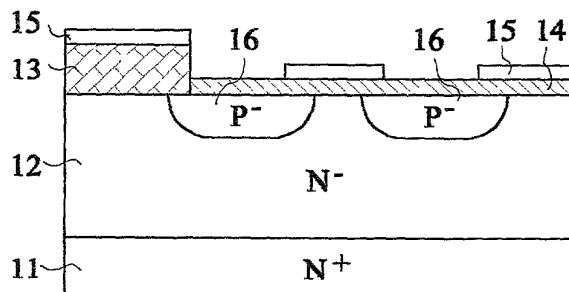
(a)



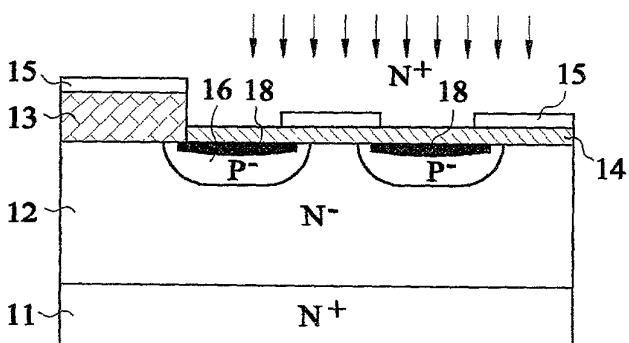
(b)



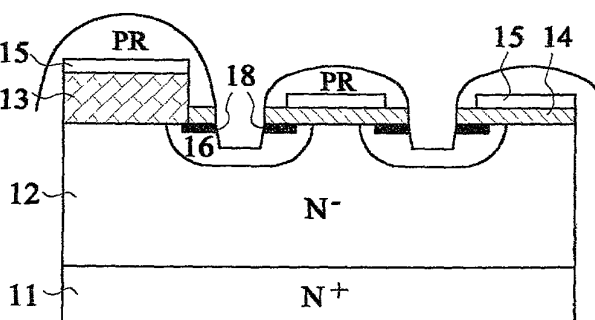
(c)



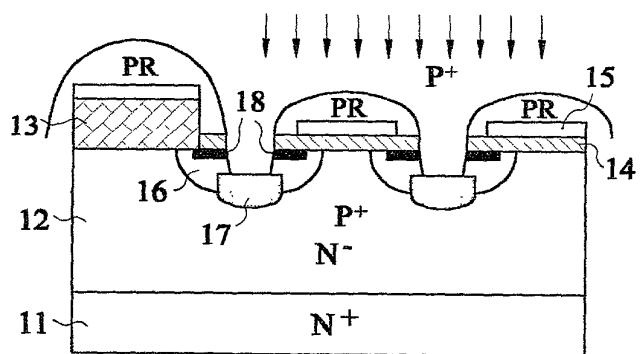
(d)



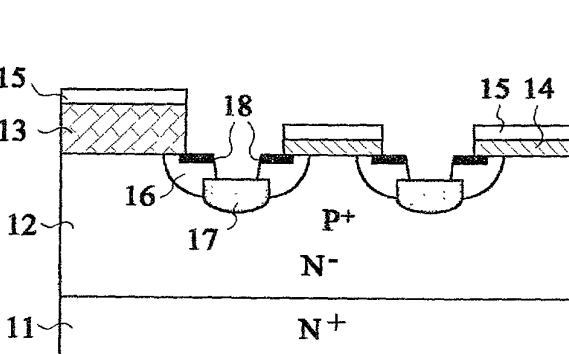
(e)



(f)

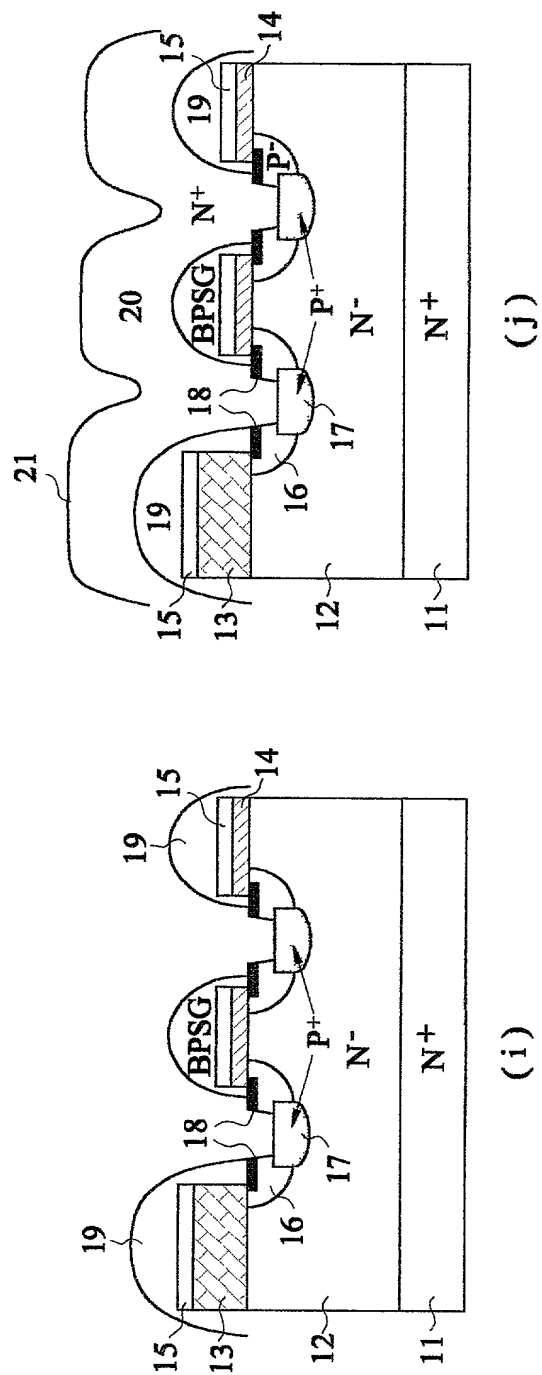


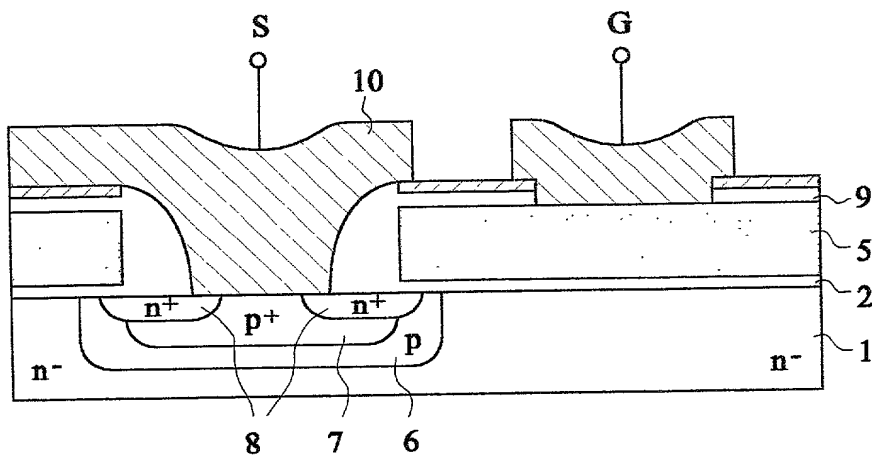
(g)



(h)

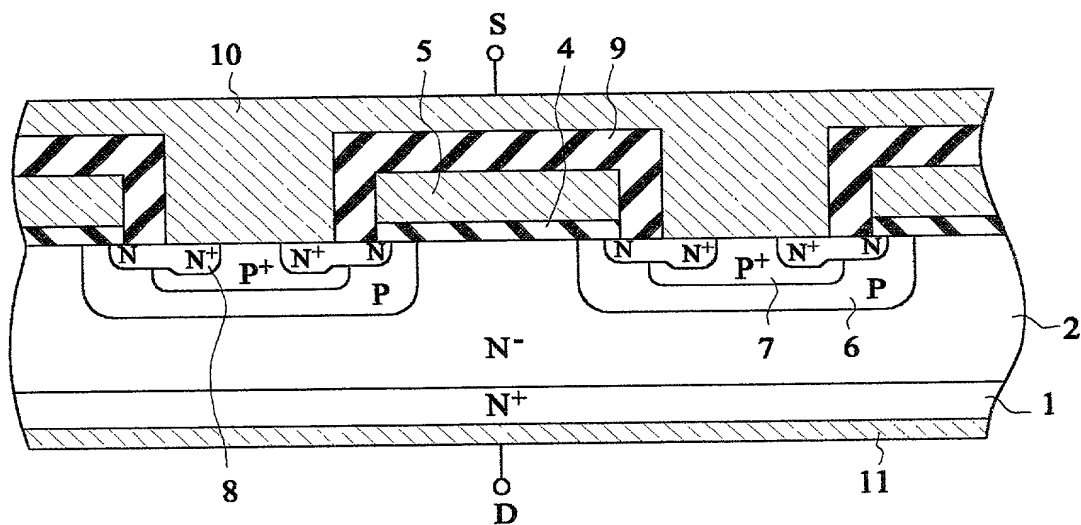
FIG. 2





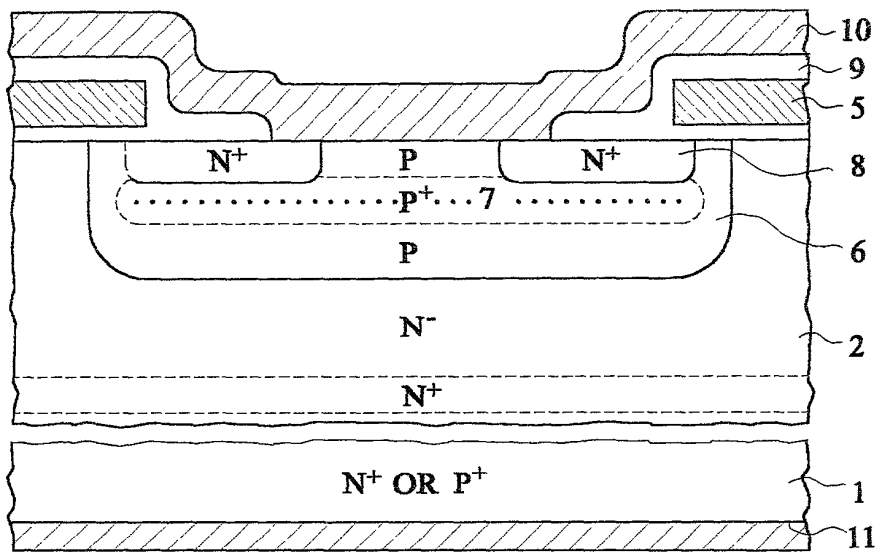
(PRIOR ART)

FIG. 3



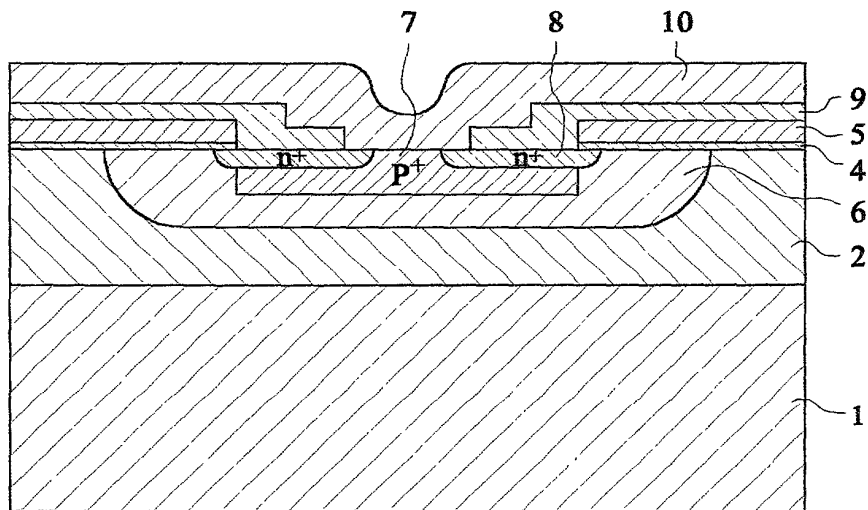
(PRIOR ART)

FIG. 4



(PRIOR ART)

FIG. 5



(PRIOR ART)

FIG. 6

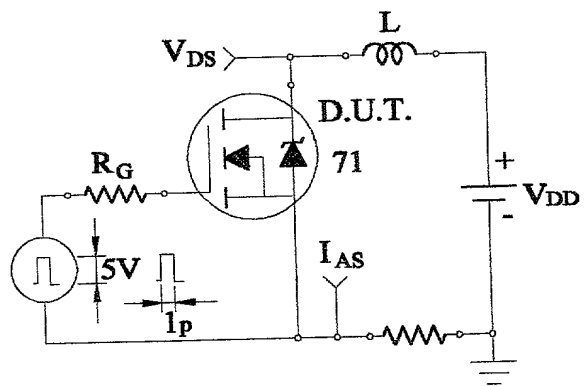


FIG. 7a

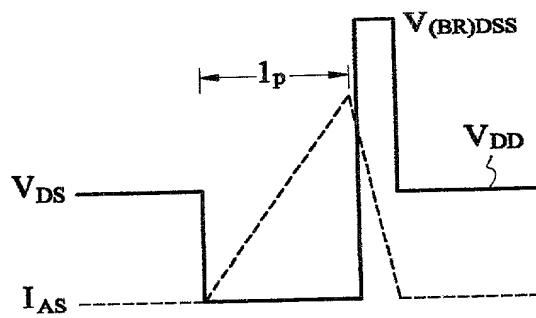


FIG. 7b

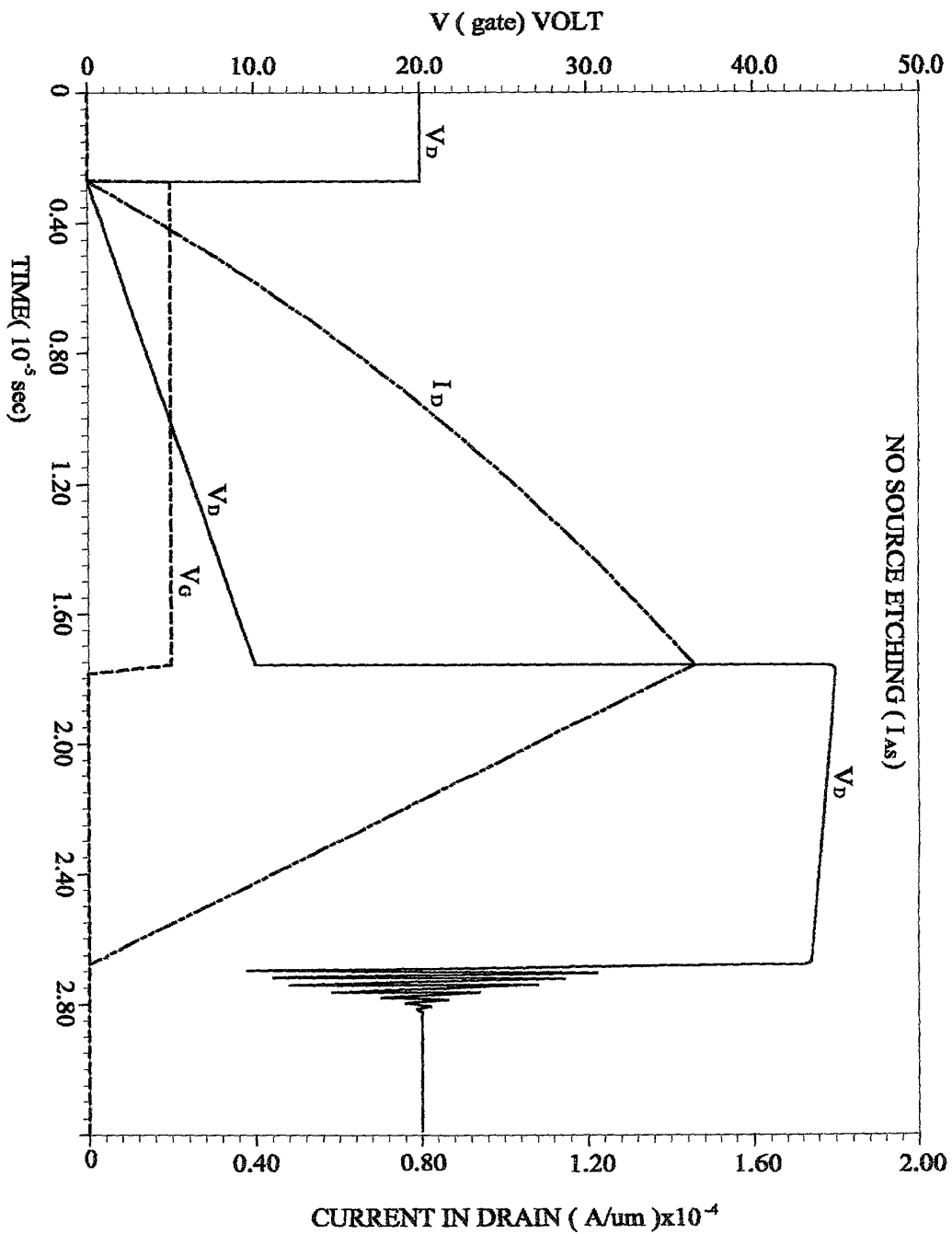


FIG. 8 (PRIOR ART)

FIG. 8 (PRIOR ART) is a graph showing the relationship between the gate voltage (V_G), the drain current (I_D), and the drain voltage (V_D) for a device with no source etching. The x-axis represents time in units of 10⁻⁵ seconds, ranging from 0 to 2.80. The y-axis represents the gate voltage (V_G) in volts, ranging from 0 to 50.0. The graph shows a ramp-up of V_D and I_D from 0 to 1.60 V and 1.60 A/um, respectively, followed by a plateau at 1.60 V and 1.60 A/um. V_G is a step function that jumps from 0 to 1.60 V at t = 0.40 x 10⁻⁵ s and remains constant thereafter.

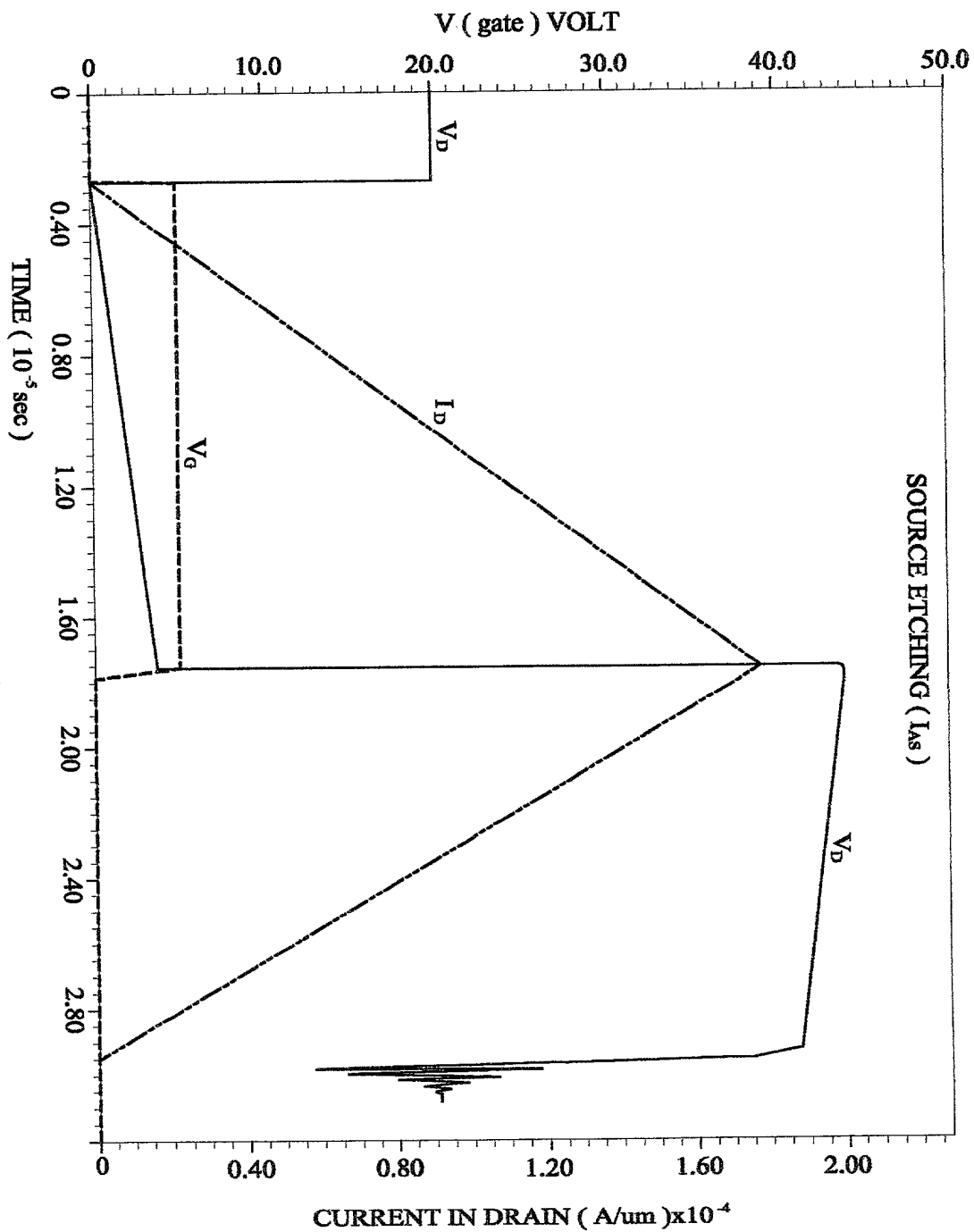


FIG. 9